NJIT | INSTITUTE FOR DATA SCIENCE

Data Science Seminar Series

Accelerating Data Science at the Edge

Viktor K. Prasanna, Ph.D.

Professor and Charles Lee Powell Chair in Engineering
University of Southern California

Date: Wednesday, October 14th, 2020
Time: 4:00 PM – 5:00 PM EDT
Location: Zoom Virtual Room
Web Link: https://njit-institute-for-data-science.eventbrite.com

Data Science has matured over the past few years with novel applications in diverse areas including health, energy, autonomous x, etc. Many of these are cyber physical social systems with strict requirements of latency, throughput and energy efficiency. In many applications, the computations need to be performed at the “edge” as the data is collected. With recent dramatic advances in Field Programmable Gate Arrays (FPGAs), these devices are being used along with multi-core and novel memory technologies to realize advanced platforms to accelerate complex applications. This talk will review our recent work in the Data Science Lab at USC (dslab.usc.edu) and advances in reconfigurable computing (fpga.usc.edu) leading up to current trends in accelerators for data science. We will illustrate FPGA-based parallel architectures and algorithms for a variety of data analytics kernels in streaming graph processing and machine learning for “edge” processing. While demonstrating algorithm-architecture co-design methodology to realize high performance accelerators for graphs and machine learning, we demonstrate the role of modeling and algorithmic optimizations to develop highly efficient Intellectual Property (IP) cores. We show improved performance for two broad classes of graph analytics: iterative graph algorithms with variable workload (e. g., graph traversal, shortest paths, etc.) and machine learning on graphs (e. g., graph embedding). For variable workload iterative graph algorithms, we illustrate dynamic algorithm adaptation to exploit heterogeneity in the architecture. For graph embedding, we develop a novel computationally efficient technique using graph sampling and demonstrate scalable performance. We conclude by identifying opportunities and challenges in exploiting emerging heterogeneous architectures composed of multi-core processors, FPGAs, GPUs and coherent memory.

Viktor K. Prasanna (ceng.usc.edu/~prasanna) is Charles Lee Powell Chair in Engineering in the Ming Hsieh Department of Electrical and Computer Engineering and Professor of Computer Science at the University of Southern California. He is the director of the Center for Energy Informatics at USC and leads the FPGA (fpga.usc.edu) and Data Science Labs (dslab.usc.edu). His research interests include parallel and distributed computing, accelerator design, reconfigurable architectures and algorithms and high performance computing. He served as the Editor-in-Chief of the IEEE Transactions on Computers during 2003-06 and is currently the Editor-in-Chief of the Journal of Parallel and Distributed Computing. Prasanna was the founding Chair of the IEEE Computer Society Technical Committee on Parallel Processing. He is the Steering Chair of the IEEE International Parallel and Distributed Processing Symposium and the Steering Chair of the IEEE International Conference on High Performance Computing. His work has received best paper awards at leading forums in parallel computing, HPC and FPGAs, including ACM/IEEE Computing Frontiers, International Parallel and Distributed Processing Symposium, ACM International Symposium on FPGAs, among others. He is a Fellow of the IEEE, the ACM and the American Association for Advancement of Science (AAAS). He is a recipient of 2009 Outstanding Engineering Alumnus Award from the Pennsylvania State University and a 2019 Distinguished Alumnus Award from the Indian Institute of Science. He received the 2015 W. Wallace McDowell award from the IEEE Computer Society for his contributions to reconfigurable computing.